Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1-14. (Canceled).

15. (Previously Presented) A semiconductor device of IGBT comprising:

an emitter electrode;

a top region of a second conductivity type connected to the emitter electrode;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type isolating the top region and the deep region;

a collector region of the first conductivity type connected to the deep region, the collector region being isolated from the intermediate region by the deep region;

a collector electrode connected to the collector region;

a gate electrode facing a portion of the intermediate region via an insulating layer, the portion of the intermediate region isolating the top region and the deep region; and

a barrier region comprising a semiconductor region of the second conductivity type formed within the intermediate region,

wherein the intermediate region comprises a dense portion directly connected to the emitter electrode, and

a main portion connected to the emitter electrode via the dense portion,

wherein the barrier region is in contact with the dense portion, and is separated from the deep region by the main portion.

16. (Previously Presented) A semiconductor device according to claim 15,

wherein the barrier region further comprises an insulator.

17. (Previously Presented) A semiconductor device according to claim 15,

wherein the thickness of the top region is less than the thickness of the barrier region.

18-19. (Canceled)

20. (Previously Presented) A semiconductor device of IGBT comprising:

an emitter electrode;

a top region of a second conductivity type connected to the emitter electrode;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type connected to the emitter electrode, the intermediate region isolating the top region and the deep region;

a collector region of the first conductivity type connected to the deep region, the collector region being isolated from the intermediate region by the deep region;

a collector electrode connected to the collector region;

a gate electrode facing a portion of the intermediate region via an insulating layer, the portion of the intermediate region isolating the top region and the deep region; and

a plurality of barrier regions, each comprising a semiconductor region of the second conductive type and formed within the intermediate region;

wherein the barrier regions are distributed within the intermediate region along a direction extending between the top region and the deep region.

21. (Currently Amended) A semiconductor device according to claim[[s]] 20,

wherein the intermediate region comprises a dense portion directly connected to the emitter electrode, and a main portion connected to the emitter electrode via the dense portion,

wherein at least one of the barrier regions is formed in the vicinity of a boundary between the dense portion and the main portion,

wherein at least another of the barrier regions is formed in the vicinity of a boundary between the main portion and the deep region, and is electrically disconnected from the emitter electrode and the deep region.

22. (Currently Amended) A semiconductor device according to claim[[s]] 21,

wherein at least a portion of each of the barrier regions is located on a path along which carriers flow.

23. (Currently Amended) A semiconductor device according to claim[[s]] 22,
wherein a plurality of pairs of barrier layer and intermediate layer is stacked.

24. (Currently Amended) A semiconductor device according to claim[[s]] 20,
wherein the intermediate region comprises a dense portion directly connected to the emitter electrode, and a main portion connected to the emitter electrode via the dense portion,
wherein at least one of the barrier regions is formed in the vicinity of a boundary between the dense portion and the main portion,
wherein at least another of the barrier regions is formed at a boundary between the main portion and the deep region, and has a higher concentration of impurities than the deep region.

25. (Currently Amended) A semiconductor device according to claim[[s]] 24,
wherein at least a portion of each of the barrier regions is located on a path along which carriers flow.

26. (Currently Amended) A semiconductor device according to claim[[s]] 25,
wherein a plurality of pairs of barrier layer and intermediate layer is stacked.

27. (Previously Presented) A semiconductor device according to claim 20,
wherein the thickness of the top region is less than the thickness of the barrier region.